The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Canceled)

2. (New) A method of manufacturing a circuit comprising:

forming first and second semiconductor layers over a substrate;

forming a gate insulating film over the first and the second semiconductor layers;

forming gate electrodes over the first and the second semiconductor layers with the gate insulating film interposed therebetween;

introducing a first impurity element into portions of the first and the second semiconductor layers so as to form first impurity regions;

introducing a second impurity element into portions of the first and the second semiconductor layers so as to form second impurity regions in contact with the first impurity regions;

introducing a third impurity element into portions of the first semiconductor layer so as to form third impurity regions in contact with the second impurity regions; and

forming wirings so as to be in contact with the third impurity regions.

3. (New) A method of manufacturing a circuit according to claim 2 wherein a concentration of the third impurity regions is higher than that of the second impurity regions, and a concentration of the second impurity regions is higher than that of the first impurity regions.

4. (New) A method of manufacturing a circuit according to claim 2 wherein the first, the second, and the third impurity elements comprise phosphorus.

5. (New) A method of manufacturing a circuit according to claim 2 wherein the circuit is a logic circuit.

6. (New) A method of manufacturing a circuit according to claim 2 wherein the circuit is incorporated in an electroluminescence display device.

7. (New) A method of manufacturing a circuit according to claim 2 wherein the circuit is incorporated in at least one selected from the group consisting of a cellular phone, a video camera, a mobile computer, a goggle-type display, a projector, and an electronic book.

8. (New) A method of manufacturing a circuit comprising:

forming first and second semiconductor layers over a substrate;

forming a gate insulating film over the first and the second semiconductor layers;

forming gate electrodes over the first and the second semiconductor layers with the gate insulating film interposed therebetween;

introducing a first impurity element into portions of the first and the second semiconductor layers so as to form first impurity regions;

introducing a second impurity element into portions of the first and the second semiconductor layers so as to form second impurity regions in contact with the first impurity regions; and

introducing a third impurity element into portions of the first semiconductor layer so as to form third impurity regions in contact with the second impurity regions,

wherein an edge of the gate insulating film is aligned with a boundary between the second impurity regions and the third impurity regions.

9. (New) A method of manufacturing a circuit according to claim 8 wherein a concentration of the third impurity regions is higher than that of the second impurity

regions, and a concentration of the second impurity regions is higher than that of the first impurity regions.

10. (New) A method of manufacturing a circuit according to claim 8 wherein the first, the second, and the third impurity elements comprise phosphorus.

11. (New) A method of manufacturing a circuit according to claim 8 wherein the circuit is a logic circuit.

12. (New) A method of manufacturing a circuit according to claim 8 wherein the circuit is incorporated in an electroluminescence display device.

13. (New) A method of manufacturing a circuit according to claim 8 wherein the circuit is incorporated in at least one selected from the group consisting of a cellular phone, a video camera, a mobile computer, a goggle-type display, a projector, and an electronic book.

14. (New) A method of manufacturing a circuit comprising:

forming first and second semiconductor layers over a substrate, wherein the first semiconductor layer has a larger width than that of the second semiconductor layer;

forming a gate insulating film over the first and the second semiconductor layers;

forming gate electrodes over the first and the second semiconductor layers with the gate insulating film interposed therebetween;

introducing a first impurity element into portions of the first and the second semiconductor layers so as to form first impurity regions;

introducing a second impurity element into portions of the first and the second semiconductor layers so as to form second impurity regions in contact with the first impurity regions; and

introducing a third impurity element into portions of the first semiconductor layer so as to form third impurity regions in contact with the second impurity regions.

15. (New) A method of manufacturing a circuit according to claim 14 wherein a concentration of the third impurity regions is higher than that of the second impurity regions, and a concentration of the second impurity regions is higher than that of the first impurity regions.

16. (New) A method of manufacturing a circuit according to claim 14 wherein the first, the second, and the third impurity elements comprise phosphorus.

17. (New) A method of manufacturing a circuit according to claim 14 wherein the circuit is a logic circuit.

18. (New) A method of manufacturing a circuit according to claim 14 wherein the circuit is incorporated in an electroluminescence display device.

19. (New) A method of manufacturing a circuit according to claim 14 wherein the circuit is incorporated in at least one selected from the group consisting of a cellular phone, a video camera, a mobile computer, a goggle-type display, a projector, and an electronic book.

20. (New) A method of manufacturing a circuit comprising:

forming first and second semiconductor layers over a substrate;

forming a gate insulating film over the first and the second semiconductor layers;

forming gate electrodes over the first and the second semiconductor layers with the gate insulating film interposed therebetween;

introducing a first impurity element into portions of the first and the second semiconductor layers so as to form first impurity regions;

introducing a second impurity element into portions of the first and the second semiconductor layers so as to form second impurity regions in contact with the first impurity regions;

introducing a third impurity element into portions of the first semiconductor layer so as to form third impurity regions in contact with the second impurity regions; and

forming wirings so as to be in contact with the third impurity regions,

wherein an edge of the gate insulating film is aligned with a boundary between the second impurity regions and the third impurity regions.

21. (New) A method of manufacturing a circuit according to claim 20 wherein a concentration of the third impurity regions is higher than that of the second impurity regions, and a concentration of the second impurity regions is higher than that of the first impurity regions.

22. (New) A method of manufacturing a circuit according to claim 20 wherein the first, the second, and the third impurity elements comprise phosphorus.

23. (New) A method of manufacturing a circuit according to claim 20 wherein the circuit is a logic circuit.

24. (New) A method of manufacturing a circuit according to claim 20 wherein the circuit is incorporated in an electroluminescence display device.

25. (New) A method of manufacturing a circuit according to claim 20 wherein the circuit is incorporated in at least one selected from the group consisting of a cellular phone, a video camera, a mobile computer, a goggle-type display, a projector, and an electronic book.

26. (New) A method of manufacturing a circuit comprising:

forming first and second semiconductor layers over a substrate, wherein the first semiconductor layer has a larger width than that of the second semiconductor layer;

forming a gate insulating film over the first and the second semiconductor layers;

forming gate electrodes over the first and the second semiconductor layers with the gate insulating film interposed therebetween;

introducing a first impurity element into portions of the first and the second semiconductor layers so as to form first impurity regions;

introducing a second impurity element into portions of the first and the second semiconductor layers so as to form second impurity regions in contact with the first impurity regions;

introducing a third impurity element into portions of the first semiconductor layer so as to form third impurity regions in contact with the second impurity regions; and

forming wirings so as to be in contact with the third impurity regions.

27. (New) A method of manufacturing a circuit according to claim 26 wherein a concentration of the third impurity regions is higher than that of the second impurity regions, and a concentration of the second impurity regions is higher than that of the first impurity regions.

28. (New) A method of manufacturing a circuit according to claim 26 wherein the first, the second, and the third impurity elements comprise phosphorus.

29. (New) A method of manufacturing a circuit according to claim 26 wherein the circuit is a logic circuit.

30. (New) A method of manufacturing a circuit according to claim 26 wherein the circuit is incorporated in an electroluminescence display device.

31. (New) A method of manufacturing a circuit according to claim 26 wherein the circuit is incorporated in at least one selected from the group consisting of a cellular

phone, a video camera, a mobile computer, a goggle-type display, a projector, and an electronic book.

32. (New) A method of manufacturing a circuit comprising:

forming first and second semiconductor layers over a substrate, wherein the first semiconductor layer has a larger width than that of the second semiconductor layer;

forming a gate insulating film over the first and the second semiconductor layers;

forming gate electrodes over the first and the second semiconductor layers with the gate insulating film interposed therebetween;

introducing a first impurity element into portions of the first and the second semiconductor layers so as to form first impurity regions;

introducing a second impurity element into portions of the first and the second semiconductor layers so as to form second impurity regions in contact with the first impurity regions;

introducing a third impurity element into portions of the first semiconductor layer so as to form third impurity regions in contact with the second impurity regions; and

forming wirings so as to be in contact with the third impurity regions,

wherein an edge of the gate insulating film is aligned with a boundary between the second impurity regions and the third impurity regions.

33. (New) A method of manufacturing a circuit according to claim 32 wherein a concentration of the third impurity regions is higher than that of the second impurity regions, and a concentration of the second impurity regions is higher than that of the first impurity regions.

34. (New) A method of manufacturing a circuit according to claim 32 wherein the first, the second, and the third impurity elements comprise phosphorus.

35. (New) A method of manufacturing a circuit according to claim 32 wherein the circuit is a logic circuit.

36. (New) A method of manufacturing a circuit according to claim 32 wherein the circuit is incorporated in an electroluminescence display device.

37. (New) A method of manufacturing a circuit according to claim 32 wherein the circuit is incorporated in at least one selected from the group consisting of a cellular phone, a video camera, a mobile computer, a goggle-type display, a projector, and an electronic book.